SEMICONDUCTOR MEMORY DEVICE

ABSTRACT OF THE DISCLOSURE

A semiconductor memory device for improving the utilization of a shared data bus and the data transfer rate in a multi-bank DRAM and realizing high speed data accessing without increasing a scale of a control circuit, wherein the multi-bank DRAM has memory banks provided with an address register for holding a write address, a data register for holding write data, an address matching detection circuit for detecting whether an address held in the address register matches with an address input this time, and when reading is performed continuously from writing on the same address of the same memory bank, reading is not performed on a memory cell specified by a read address and data held in the data register is output as read data, so that memory accessing made continuously to the same address can be performed at a high speed.